IN THE SPECIFICATION:

Please replace paragraph [0015] as follows:

[0015] The sources ~~drains~~ of PM0 and PM1 are connected to a high operating voltage VDDH, which is typically higher than a regular operating voltage, for the reason previously described. For example, VDDH is 3.3V and the threshold voltage to achieve hot carrier effect is 1.2V, while regular operating voltage is less than 1V. The drains ~~sources~~ of PM0 and PM1 are connected to both the gates and drains of NM2 and NM3, respectively, and further connected to the sources of NM0 and NM1, respectively. For illustration purposes, control voltage levels/references at the drains ~~sources~~ of PM0 and PM1 are referred to as V0 and V1, respectively. Similarly, the two nodes VW0 and VW1 represent the gates of PM0 and PM1 , respectively, for programming the memory device.

Please replace paragraph [0016] as follows:

[0016] The sources of NM2 and NM3 are connected to a control voltage level such as VSS which, depending on circuit setup, may or may not be directly connected to ground. The gates of NM0 and NM1 are connected together, the connection of which has a voltage reference VR. The drain of NM0 connects to the gates of PM2 and NM4, while the drain of NM1 connects to the gates of PM3 and NM5. NM0 and NM1 can be together viewed as a connection module which passes V0 and V1 as two inputs to the latch 102 when VR is set at an appropriate level. The sources ~~drains~~ of PM2 and PM3 are connected to an operating voltage VDDL, while the drains ~~sources~~ of PM2 and PM3 are connected to the drains of NM4 and NM5, respectively. The sources of NM4 and NM5 are connected to VSS. The gates of PM2 and NM4 are connected to the drain ~~source~~ of PM3 and the drain of NM5, whereupon this connection has an output voltage reference OUT. The gates of PM3 and NM5 ~~NM4~~ are connected to the drain ~~source~~ of PM2 and the drain of NM4, whereupon this connection has an output voltage reference OUTz.

Please replace paragraph [0018] as follows:

[0018] FIG. 2B illustrates a timing diagram showing the voltage at various nodes in FIG. 1 during a read operation. With reference to both FIGS. 1 and 2B, when a read operation occurs, VR rises, which is represented by a rising edge 208 ~~210~~. It is noted that before a reading

operation occurs, both OUT and OUTz are still indeterminate. When VR rises enough, NM0 and NM1 conduct, thereby sending V0 and V1 to OUT and OUTz, respectively. In this example, OUT, which carries V0, is higher than OUTz, which carries V1. As such, OUT will move to as high a voltage as VDDL, as represented by a rising edge 212, while OUTz stays at VSS. The data of the memory device can be obtained by reading OUT, which essentially carries the "1" that is originally programmed into NM2. Based on the function of the latch 102 in this configuration, it can be viewed as a comparison circuit which compares V0 and V1, and produces an output on OUT node accordingly.

Please replace paragraph [0022] as follows:

[0022] FIG. 3B illustrates a timing diagram showing the voltage at various nodes in FIG. 1 during a read operation in the second example. With reference to both FIGS. 1 and 3B, when a read operation occurs, VR rises, which is represented by a rising edge 308 ~~310~~. It is noted that before a reading operation occurs, both OUT and OUTz are still indeterminate. When VR rises enough, NM0 and NM1 conduct, thereby sending V0 and V1 to OUT and OUTz, respectively. In this example, OUT, which carries V0, is lower than OUTz, which carries V1. As such, OUTz will move to as high a voltage as VDDL, as represented by a rising edge 314 ~~312~~, while OUT stays at VSS. The data of the memory device can be obtained by reading OUT, which as represented by a falling edge 316 essentially carries the "0" since V0 is lower relative to V1 because the resistance at NM3 is higher relative to NM2.